

## DDR Termination Regulator

### *Purpose*

The RT2568 is a sink/source tracking termination regulator. This document explains the function and use of the RT2568 evaluation board (EVB), and provides information to enable operation, modification of the evaluation board and circuit to suit individual requirements.

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## Introduction

### General Product Information

The RT2568 is a sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RT2568 possesses a high speed operating amplifier that provides fast load transient response and only requires a minimum 10 $\mu$ F x 3 ceramic output capacitor. The RT2568 supports remote sensing functions and all features required to power the DDRIII and Low Power DDRIII/DDRIV VTT bus termination according to the JEDEC specification. In addition, the RT2568 provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications. The RT2568 is available in the thermal efficient package, WDFN-10L 3x3.

### Product Feature

- VIN Input Voltage Range : 1.1V to 3.5V
- VCNTL Input Voltage Range : 2.9V to 5.5V
- Support Ceramic Capacitors
- Power Good Indicator
- 10mA Source/Sink Reference Output
- Meet DDRI, DDRII JEDEC Spec
- Support DDRIII, Low Power DDRIII/DDRIV VTT Applications
- Soft-Start Function
- UVLO and OCP Protection
- Thermal Shutdown

## Applications

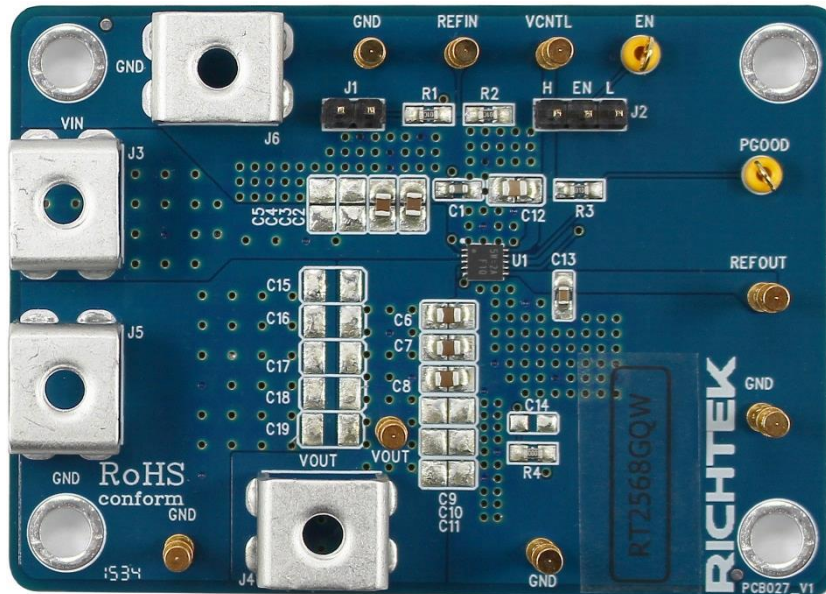
- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDPTV, Copier/Printer, Set-Top Box

## Key Performance Summary Table

Key Features	Evaluation Board Number : PCB027_V1
Input Voltage Range	1.1V to 3.5V
VCNTL Input Voltage Range	2.9V to 5.5V
Max Output Current	3A
Default Output Voltage	Set by REFIN pin voltage level ( $V_{OUT} = V_{REFIN}$ )
Default Marking & Package Type	RT2568GQW, WDFN-10L 3x3

## Bench Test Setup Conditions

### Headers Description and Placement



Please carefully inspect the EVB IC and external components, comparing them to the following Bill of Materials, to ensure that all components are installed and undamaged. If any components are missing or damaged during transportation, please contact the distributor or send e-mail to [evb\\_service@richtek.com](mailto:evb_service@richtek.com)

### Test Points

The EVB is provided with the test points and pin names listed in the table below.

Test point/ Pin name	Signal	Comment (expected waveforms or voltage levels on test points)
<b>VIN</b>	Input voltage	Input voltage range = 2.9V to 5.5V
<b>VOUT</b>	Output voltage	Power output of the regulator.
<b>EN</b>	Enable test point	Enable Control Input. EN = High (higher than 1.7V) for ON operation, while EN = Low (lower than 0.3V) for OFF operation.
<b>GND</b>	Ground	Ground.
<b>VCNTL</b>	Control voltage input	Control voltage input. Connect this pin to the 3.3V or 5V power supply. A ceramic decoupling capacitor with a value 4.7 $\mu$ F is required.
<b>REFIN</b>	Reference input	Reference input.
<b>REFOUT</b>	Reference output	Reference output. Connect to GND through a 0.1 $\mu$ F ceramic capacitor.
<b>PGOOD</b>	Power good output test point	Power good open-drain output. Connect a pull-up resistor between this pin and VCNTL pin.

### **Power-up & Measurement Procedure**

1. Short J1 and the (1, 2) pin of J2 by jumper respectively.
2. Provide input voltage ( $2.9V < V_{CNTL} < 5.5V$ ) to VCNTL pin.
3. Connect input power ( $1.1V < V_{IN} < 3.5V$ ) and input ground to VIN and GND pins respectively.
4. Connect positive end and negative end of load to VOUT and GND of output pins respectively.
5. The output voltage of ( $V_{OUT}$ ) can be set by R1 and R2 :

$$V_{OUT} = V_{IN} \times \left( \frac{R2}{R1 + R2} \right)$$

6. If J1 is not shorted by Jumper, the output voltage can be set by the input voltage of REFIN pin :

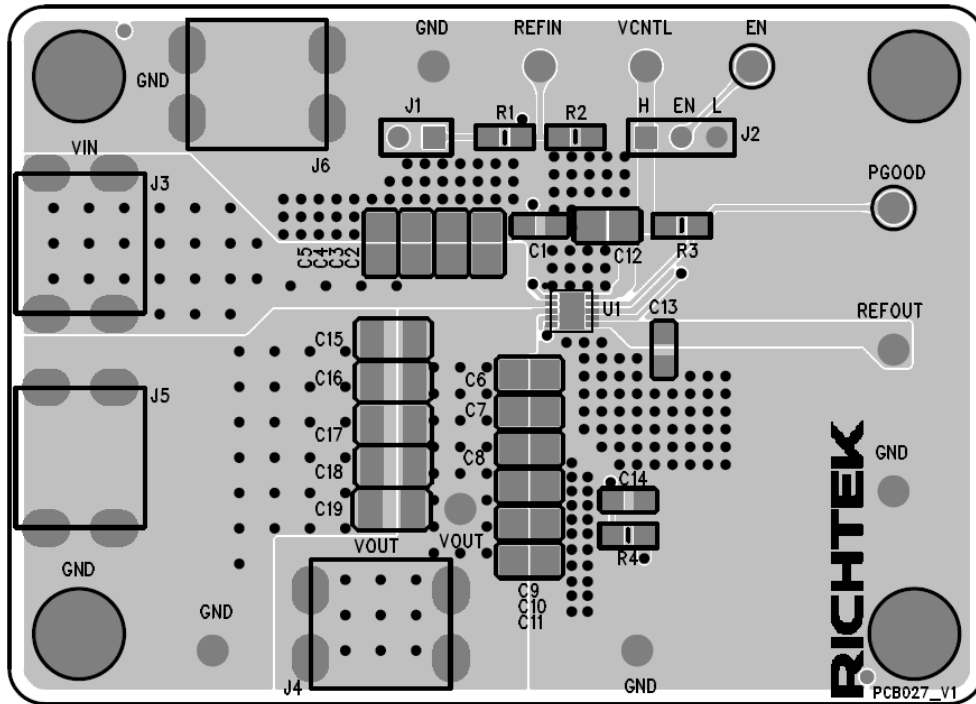
$$V_{OUT} = V_{REFIN}$$

### **Specification**

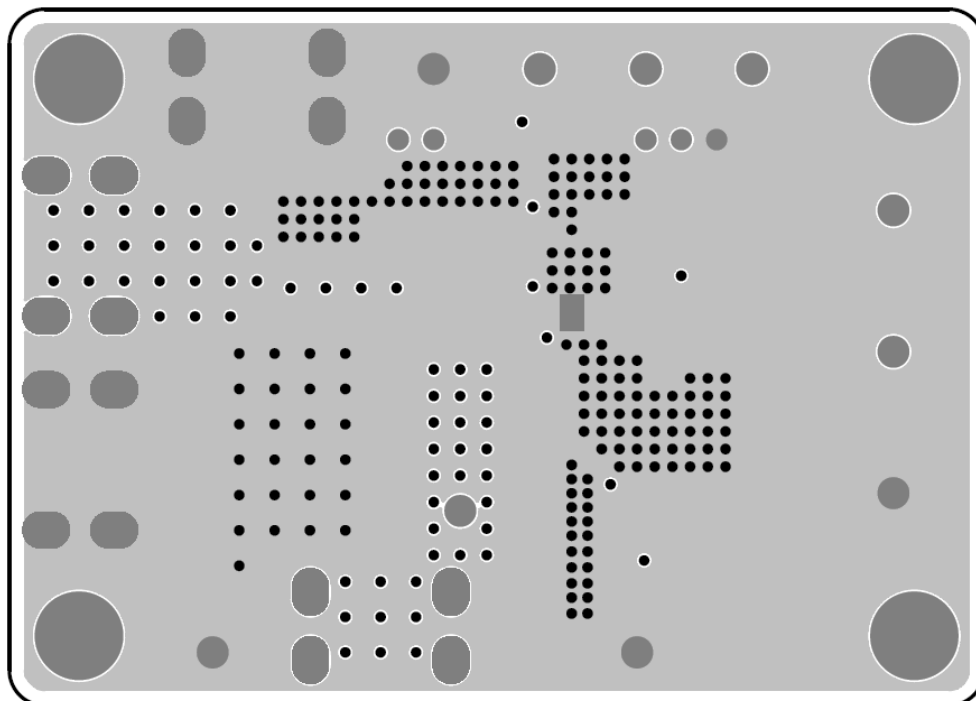
Parameter	Symbol	Min	Typ.	Max	Units
Control Input Voltage	VCNTL	2.9		5.5	V
Supply Input Voltage	VIN	1.1		3.5	V
VOUT Source Current Limit	I <sub>LIM_VOUT_SR</sub>	3.5		5.5	A
VOUT Sink Current Limit	I <sub>LIM_VOUT_SK</sub>	3.5		5.5	A
REFIN Voltage Range	VREFIN	0.5		1.8	V



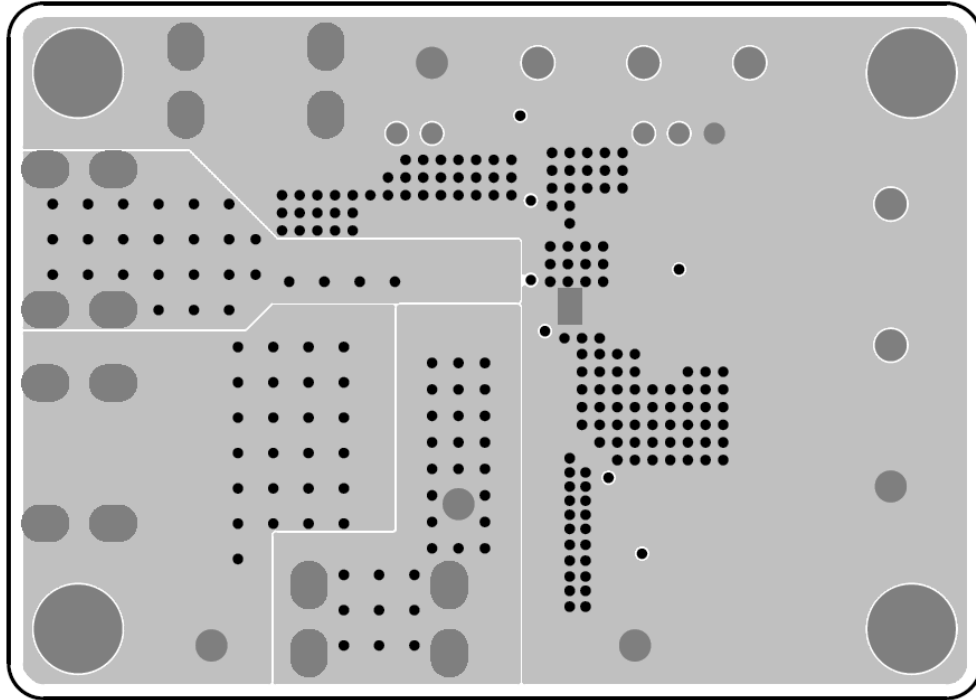
**PCB Layout**



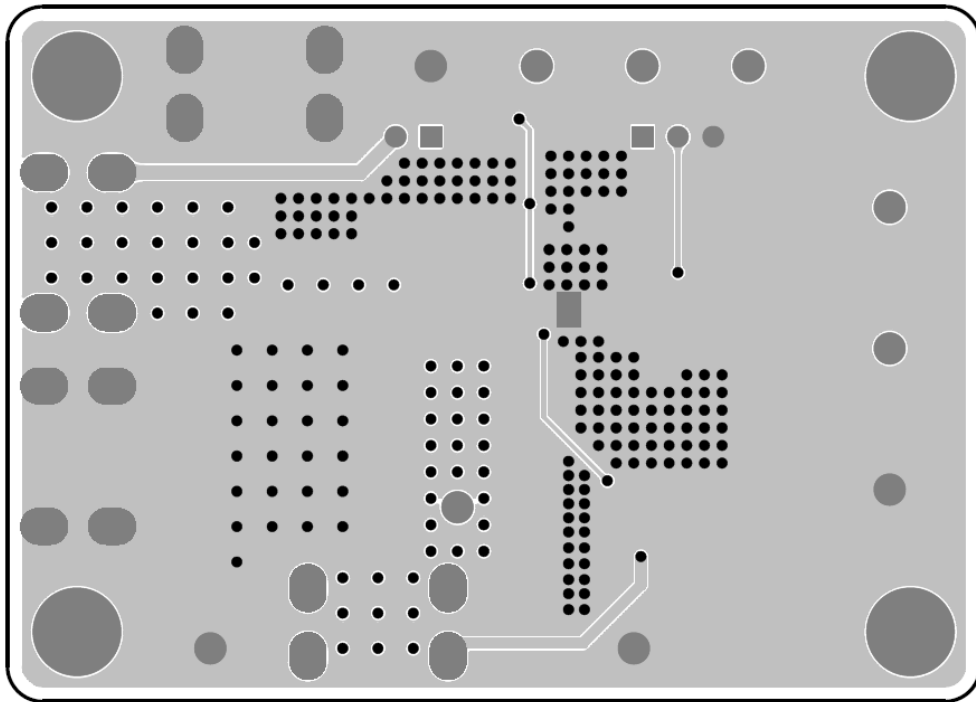
Top View (1<sup>st</sup> layer)



PCB Layout—Inner Side (2<sup>nd</sup> Layer)



PCB Layout—Inner Side (3<sup>rd</sup> Layer)



Bottom View (4<sup>th</sup> Layer)

### ***More Information***

For more information, please find the related datasheet or application notes from Richtek website <http://www.richtek.com>.

### ***Important Notice for Richtek Evaluation Board***

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